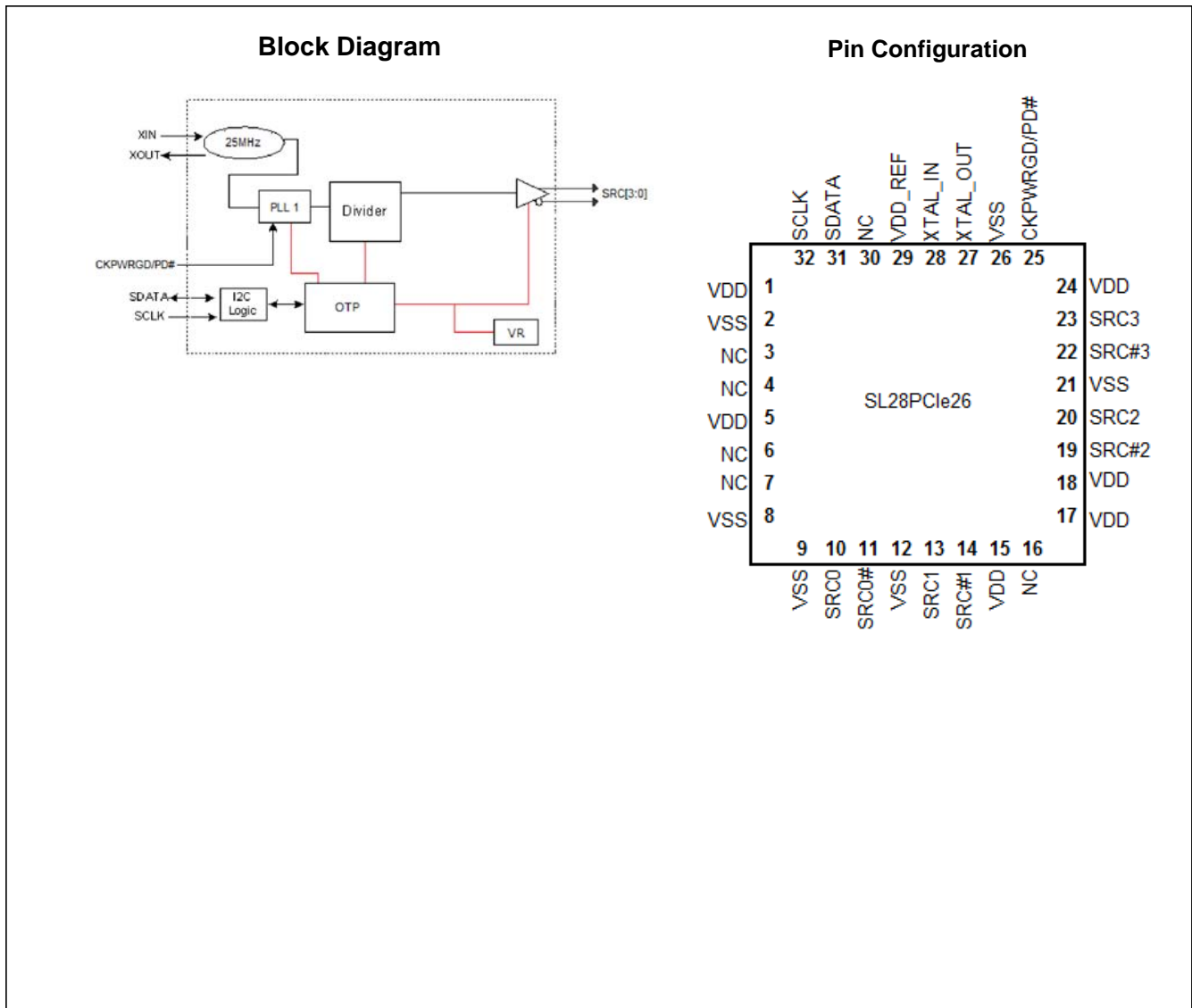


PC EProClock[®] PCI Express Gen 2 & Gen 3 Generator

Features

- Optimized 100 MHz Operating Frequencies to Meet the Next Generation PCI-Express Gen 2/Gen 3
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Four 100-MHz differential SRC clocks
- Low jitter (<50ps)
- Input frequency of 25MHz
- PC EProClock[®] Programmable Technology
- I²C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 32-pin QFN package



32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	VDD	PWR	3.3V Power Supply
2	VSS	GND	Ground
3	NC	NC	No Connect.
4	NC	NC	No Connect.
5	VDD	PWR	3.3V Power Supply
6	NC	NC	No Connect.
7	NC	NC	No Connect.
8	VSS	GND	Ground
9	VSS	GND	Ground
10	SRC0	O, DIF	100MHz True differential serial reference clock
11	SRC0#	O, DIF	100MHz Complement differential serial reference clock
12	VSS	GND	Ground
13	SRC1	O, DIF	100MHz True differential serial reference clock
14	SRC1#	O, DIF	100MHz Complement differential serial reference clock
15	VDD	PWR	3.3V Power Supply
16	NC	NC	No Connect.
17	VDD	PWR	3.3V Power Supply
18	VDD	PWR	3.3V Power Supply
19	SRC2	O, DIF	100MHz True differential serial reference clock
20	SRC2#	O, DIF	100MHz Complement differential serial reference clock
21	VSS	GND	Ground
22	SRC3	O, DIF	100MHz True differential serial reference clock
23	SRC3#	O, DIF	100MHz Complement differential serial reference clock
24	VDD	PWR	3.3V Power Supply
25	CK_PWRGD/PD#	I	3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FS. After CK_PWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW)
26	VSS	GND	Ground
27	XOUT	O, SE	25MHz Crystal output
28	XIN	I	25MHz Crystal input
29	VDD	PWR	3.3V Power Supply
30	NC	NC	No Connect.
31	SDATA	I/O	SMBus compatible SDATA
32	SCLK	I	SMBus compatible SCLOCK

PC EProClock® Programmable Technology

PC EProClock® is the world's first non-volatile programmable PC clock. The PC EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

PC EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate
- For more information: Please refer to Application Note #25

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address--7 bits	8:2	Slave address--7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code--8 bits	18:11	Command Code--8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count--8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address--7 bits
36:29	Data byte 1--8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2--8 bits	37:30	Byte Count from slave--8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave--8 bits
....	Data Byte N--8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave--8 bits
....	Stop	56	Acknowledge
		Data bytes from slave / Acknowledge

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
		Data Byte N from slave–8 bits
		NOT Acknowledge
		Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers
Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	PLL1_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	SRC0_OE	Output enable for SATA 0 = Output Disabled, 1 = Output Enabled
5	1	SRC1_OE	Output enable for SRC 0 = Output Disabled, 1 = Output Enabled
4	0	RESERVED	RESERVED
3	1	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
2	1	SRC2_OE	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
1	0	PLL1_SS_EN	Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
0	1	RESERVED	RESERVED

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	1	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	0	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2

Byte 7: Vendor ID

1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	1	Device_ID3	RESERVED
6	0	Device_ID2	RESERVED
5	0	Device_ID1	RESERVED
4	0	Device_ID0	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	TEST_MODE_SEL	Test mode select either REF/N or tri-state 0 = All outputs tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allows entry into test mode 0 = Normal Operation, 1 = Enter test mode(s)
2	1	I2C_VOUT<2>	Amplitude configurations differential clocks I2C_VOUT[2:0] 000 = 0.30V 001 = 0.40V 010 = 0.50V 011 = 0.60V 100 = 0.70V 101 = 0.80V (default) 110 = 0.90V 111 = 1.00V
1	0	I2C_VOUT<1>	
0	1	I2C_VOUT<0>	

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED

Byte 11: Control Register 11 (continued)

6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 12: Byte Count

Bit	@Pup	Name	Description
7	0	BC7	Byte count register for block read operation. The default value for Byte count is 15. In order to read beyond Byte 15, the user should change the byte count limit to or beyond the byte that is desired to be read.
6	0	BC6	
5	0	BC5	
4	0	BC4	
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	Wireless Friendly mode	Wireless Friendly Mode 0 = Disabled, Default all single-ended clocks slew rate config bits to '101' 1 = Enabled, Default all single-ended clocks slew rate config bits to '111'

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	OTP_4	OTP_ID Identification for programmed device
3	0	OTP_3	
2	1	OTP_2	
1	0	OTP_1	
0	1	OTP_0	

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
25 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SL28PCle26 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the SL28PCle26 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

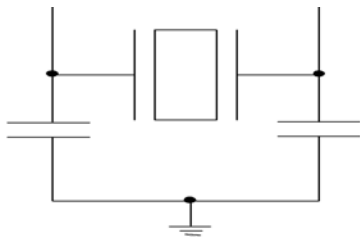


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

PD# (Power down) Assertion

When PD# is sampled HIGH by two consecutive rising edges

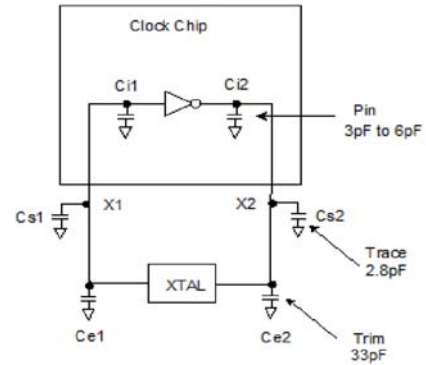


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL..... Crystal load capacitance
- CLe..... Actual loading seen by crystal using standard value trim capacitors
- Ce..... External trim capacitors
- Cs..... Stray capacitance (terraced)
- Ci Internal capacitance (lead frame, bond wires, etc.)

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

of SRC clocks , all differential clocks must held LOW. When PD# mode is desired as the initial power on state, PD# must

be asserted HIGH in less than 10 μ s after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state

condition, resulting from are driven high in less than 300 μ s of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 4* is an example showing the relationship of clocks coming up.

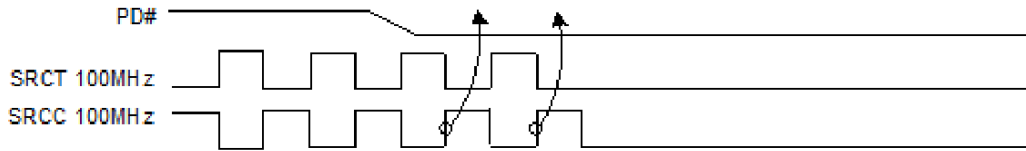


Figure 3. Power Down Assertion Timing Waveform

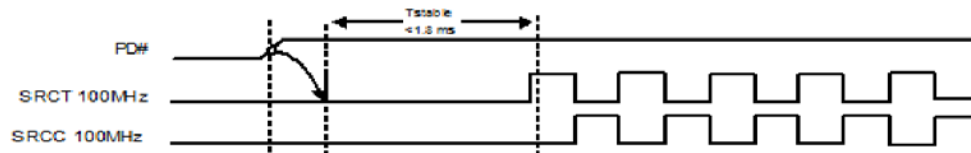


Figure 4. Power Down Deassertion Timing Waveform

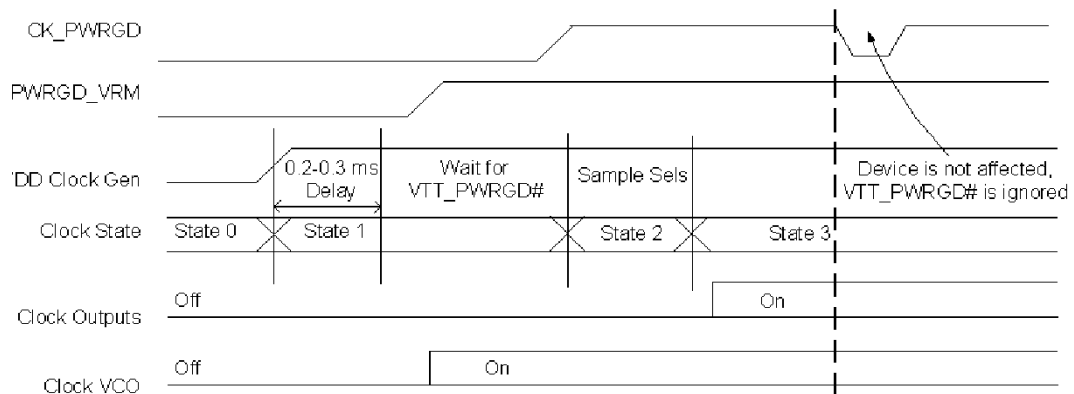


Figure 5. CK_PWRGD Timing Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD_3.3V}	Main Supply Voltage		–	4.6	V
V _{IN}	Input Voltage	Relative to V _{SS}	–0.5	4.6	V _{DC}
T _S	Temperature, Storage	Non-functional	–65	150	°C
T _A	Temperature, Operating Ambient	Functional	–40	85	°C
T _J	Temperature, Junction	Functional	–	150	°C
∅ _{JC}	Dissipation, Junction to Case	MIL-STD-883E Method 1012.1	–	20	°C/W
∅ _{JA}	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD _{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V _{IH}	3.3V Input High Voltage (SE)		2.0	V _{DD} + 0.3	V
V _{IL}	3.3V Input Low Voltage (SE)		V _{SS} – 0.3	0.8	V
V _{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V _{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
I _{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V _{IN} < V _{DD}	–	5	μA
I _{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V _{IN} < V _{DD}	–5	–	μA
V _{OH}	3.3V Input High Voltage (DIFF)		0.70	0.90	V
V _{OL}	3.3V Input Low Voltage (DIFF)			0.40	V
I _{OZ}	High-impedance Output Current		–10	10	μA
C _{IN}	Input Pin Capacitance		1.5	5	pF
C _{OUT}	Output Pin Capacitance			6	pF
L _{IN}	Pin Inductance		–	7	nH
V _{XIH}	Xin High Voltage		0.7V _{DD}	V _{DD}	V
V _{XIL}	Xin Low Voltage		0	0.3V _{DD}	V
I _{DD_PD}	Power Down Current		–	1	mA
I _{DD_3.3V}	Dynamic Supply Current	Differential clocks with 7" traces. Loading per the CK505 spec.	–	50	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T _{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T _{PERIOD}	XIN Period	When XIN is driven from an external clock source			ns
T _R /T _F	XIN Rise and Fall Times	Measured between 0.3V _{DD} and 0.7V _{DD}	–	10.0	ns
T _{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1- μ s duration	–	500	ps
SRC at 0.7V					
T _{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T _{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
T _{PERIODSS}	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
T _{PERIODAbs}	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
T _{PERIODSSAbs}	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
T _{SKEW(window)}	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T _{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
RMS _{GEN1}	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS _{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS _{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
RMS _{GEN3}	Output phase jitter impact – PCIe* Gen3	Includes PLL BW 2 - 4 MHz, CDR = 10MHz)	0	1.0	ps
L _{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T _R / T _F	SRC Rising/Falling Slew Rate	Measured differentially from \pm 150 mV	2.5	8	V/ns
T _{RFM}	Rise/Fall Matching	Measured single-endedly from \pm 75 mV	–	20	%
V _{HIGH}	Voltage High			1.15	V
V _{LOW}	Voltage Low		–0.3	–	V
V _{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
ENABLE/DISABLE and SET-UP					
T _{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T _{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up
For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

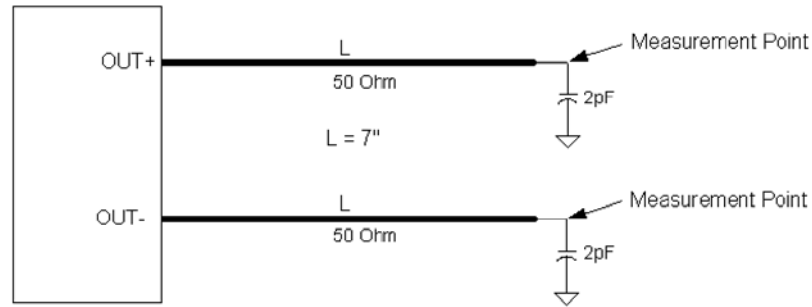


Figure 6. 0.7V Differential Load Configuration

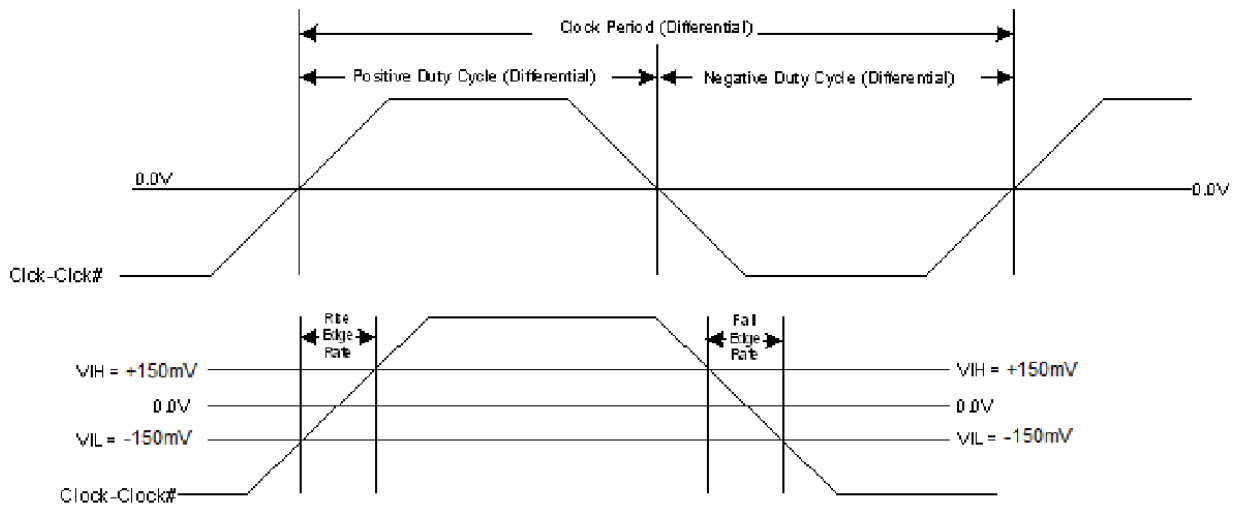


Figure 7. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

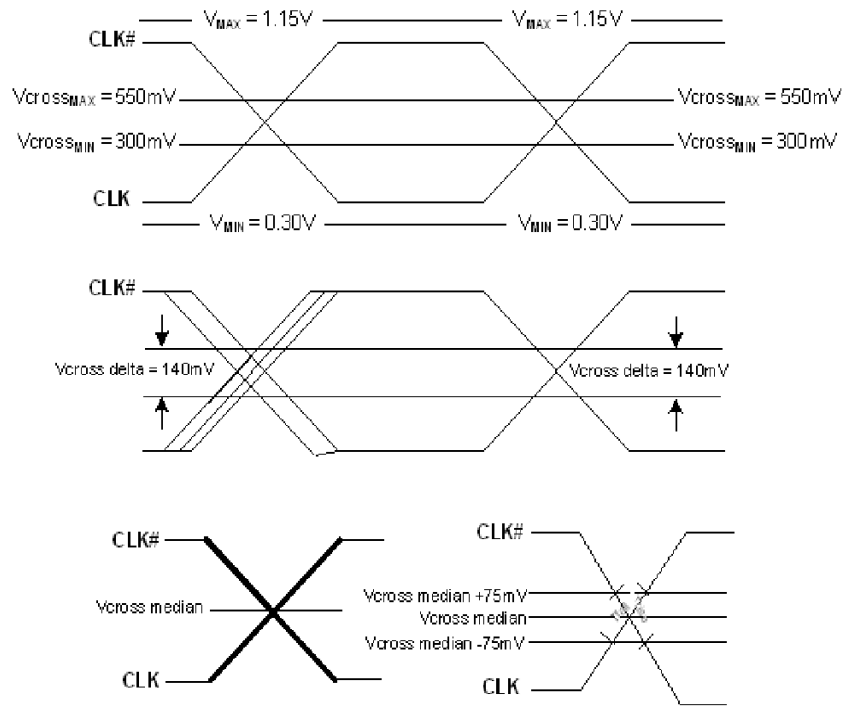
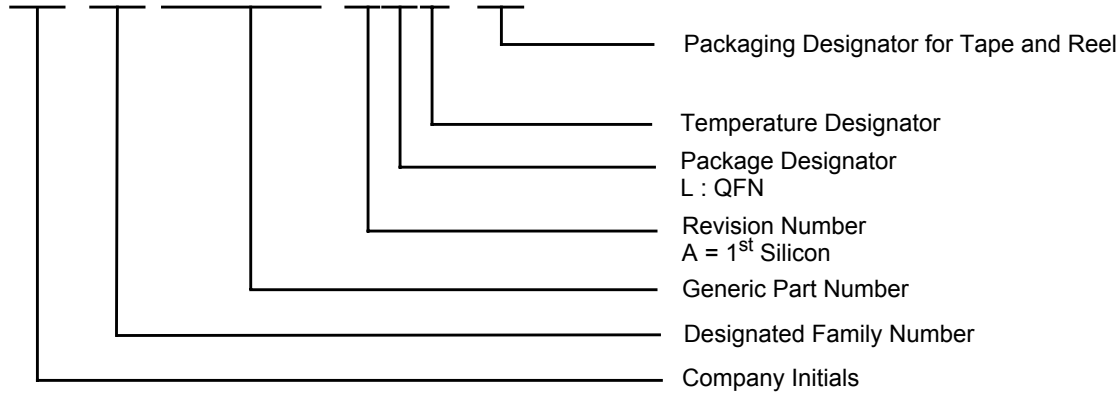


Figure 8. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28PCIe26ALI	32-pin QFN	Industrial, -40° to 85°C
SL28PCIe26ALIT	32-pin QFN–Tape and Reel	Industrial, -40° to 85°C

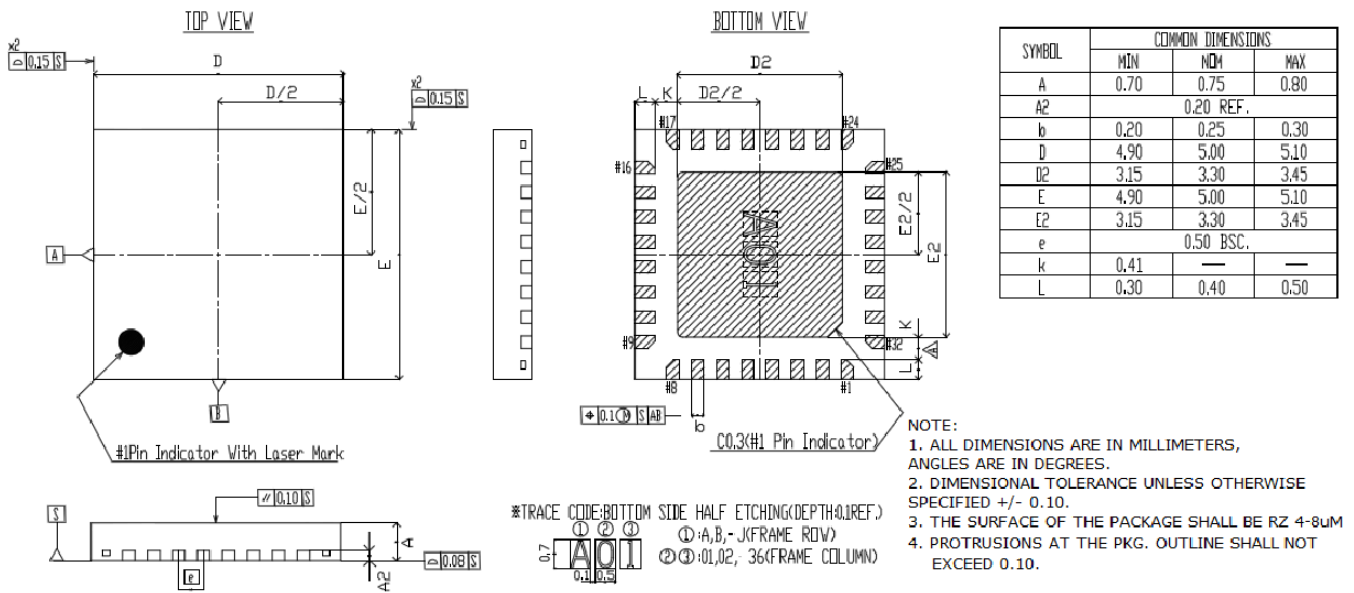
SL 28 PCIe26 ALI - T



This device is Pb free and RoHS compliant.

Package Diagrams

32-Lead QFN 5x 5mm (Saw Version)



Document History Page

Document Title: SL28PCle26 PC EProClock® PCI Express Gen 2 & Gen 3 Generator			
REV.	Issue Date	Orig. of Change	Description of Change
1.0	9/17/09	JMA	Initial Release
1.1	10/13/09	JMA	Replaced SS_EN pin with No Connect
1.2	11/25/09	JMA	Removed VDDIO Spec Removed REF specification Removed FS specification Removed Preliminary Wording Removed VOH/VOL for SE clocks Removed CPU_STP# table Updated Figure 7 Updated Pin 30 pin definition to NC Updated Figure 3, 4, and 5 Updated Register set Updated Crystal Input Spec

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